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(54) Method and system for semiconductor wafer fabrication process real-time in-situ supervision

(57) Method and system for real-time in-situ supervision of a step performed in a processing tool during semiconductor wafer fabrication. For this step, an appropriate process parameter has been selected as being the most representative of normal operating conditions. The evolutions of said selected process parameter in normal operating conditions and in all its known deviations identified by process engineers are coded and stored in a database. Analysis rules including rejection criteria adapted to recognize any such identified deviation are defined by process engineers and coded in the form of algorithms and likewise stored in the database. Finally, an alert code and the right action to be taken are also established by process engineers for each identified deviation and coded in the database. During wafer processing, this process parameter is continuously monitored, for instance by an Etch End Point (EPD) controller. The signal is coded then analyzed by a supervisor to be compared with corresponding data stored in the database in real-time. If an anomaly, i.e. a deviation to the normal process, is detected, the corresponding alert code is flagged and the recommended action immediately taken. As a result, only "good" wafers will be completely processed. This technique allows total clusterized wafer fabrication processes.

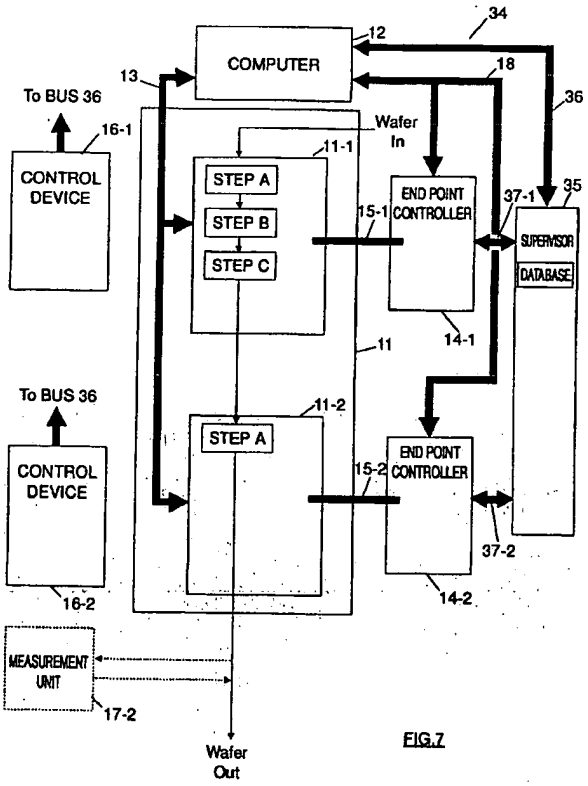

FIG.7

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Description

FIELD OF INVENTION

[0001] The present invention relates to the manufacture of semiconductor integrated circuits and more particularly to a method and a system for real-time in-situ supervision of the semiconductor wafer fabrication process. Referring to a specific processing step of the wafer fabrication process (etch, deposition, ...), by real-time in-line supervision, it is basically meant a method which includes the steps of permanently monitoring a plurality of selected process parameters in parallel during the current step, comparing their evolution with the corresponding data describing the process step when correctly performed and the identified defective deviations thereof that are stored in a database. The analysis rules developed to perform that comparison and associated rejection criteria defined by process engineers are coded in the form of algorithms and likewise stored in the database. If a process deviation is detected, an alert code is flagged to signal an alarm and the adequate action is immediately taken. The alert code is also stored in the database. A supervisor connected to the controller which monitors the processing step in consideration and to the said database is required to implement the method of the present invention.

BACKGROUND OF THE INVENTION

[0002] Due to the constant integration density increase, the fabrication processes that are used to date in the manufacture of semiconductor wafers for the production of integrated circuits (ICs) have to be very accurately controlled. For this reason, processing tools which are required to that end, are becoming more and more complex. A processing tool can include a plurality of chambers, and in turn, each chamber can run a great number of processing steps. For money saving and high throughputs, the wafer is generally processed in sequence via said plurality of chambers of the tool under computer control. The selection of the chamber depends on a number of factors such as: availability, contamination level, specialization, ... etc.

[0003] New methods for tool and process characterization such as in-situ contamination monitoring, measurements, gas analysis and the like, are now of common use in the semiconductor industry. All these characterization techniques produce huge quantity of data of various types. In particular such data include the physical process parameters such as: gas flows, pressures, RF powers, temperatures, and the like, that are permanently under computer control during a determined step. Other data include results provided by controllers (e.g. etch rates) which continuously monitor the process and by measurement units. All these data that are of paramount importance for the current step have not been effectively exploited so far.

[0004] As a matter of fact, to date, only physical process parameters are temporarily stored in the tool computer. These data are sometimes exploited for further analysis/investigations at the end of the process but they have never been used so far in real-time and in-situ for the benefit of the wafer under processing.

[0005] Fig. 1 schematically shows a conventional system of the prior art referenced 10 that implements a typical process flow for processing semiconductor wafers. The description which follows will be made by reference to a multi-chamber RIE tool such as the AME 5000 manufactured by Applied Materials, Santa Clara, CA, USA, that is adapted to perform a sequence of steps for etching different materials at the surface of the wafer. However, other tools such as deposition equipments and the like may be envisioned as well. Now turning to Fig. 1, system 10 is thus comprised of such a RIE etching tool 11 with a tool computer 12 associated thereto. As apparent from Fig. 1, tool 11 is only comprised of two chambers 11-1 and 11-2 for sake of simplicity, but in reality, it must be understood that it may have more, for instance, up to six independent chambers. Still for sake of simplicity, we will assume that each chamber performs the same sequence of processing steps, labelled A, B, ..., I, ..., X. A data bus referenced 13 provides the electrical connection between the tool chambers and the computer 12 for data flow exchange therebetween.

[0006] At initialization, computer 12 down-loads the physical process parameters of step A into chamber 11-1 or 11-2 as appropriate. Typical physical process parameters are gas flows, pressures, RF powers, temperatures and the like. Then, step A is performed and is generally stopped after a fixed time. This procedure applies for the other steps B, C, ... X, whenever necessary. During these steps, computer 12 checks the different physical process parameters via data bus 13 for process control and only stops the current process if one of them passes beyond a predefined limit. A stop generally occurs after a serious hardware failure such as a RF power shut-down or a gas flow missing.

[0007] Figure 2 describes an improved version of the system depicted in Fig. 1 now referenced 10', the same elements bearing the same references. For sake of illustration, only three (A to C) and one (A) processing steps are performed in chambers 11-1 and 11-2 respectively. In addition to the tool 11, the computer 12 and the data bus 13 connected therebetween, the improved system 10' includes additional equipments associated to each tool chamber. As apparent in Fig. 2, two etch endpoint detection (EPD) controllers 14-1 and 14-2 are provided with optical fibers 15-1 and 15-2 to view the plasma inside chambers 11-1 and 11-2 respectively. The role of these EPD controllers is only to perform optical/interferometric measurements. An adequate EPD controller that can be used in system 10' is the DIGISEM or DIGITWIN sold by SOFIE Instr., Arpajon, FRANCE. However, in the present application, "EPD" denotes either "etch end point detection" or more gener-

ally "end point detection", for instance if a deposition process is used instead of an etch process. Likewise, two control devices 16-1 and 16-2, typically particle counters, gas detectors, mass spectrometers and the like are associated to chambers 11-1 and 11-2 respectively. The nature of these control devices depends on the function: etching, deposition, ... of the tool in consideration. Control devices are used by the operators for visual inspection of the on-going process, so that they may stop it in case of need, for instance, if a contamination in excess is detected by a particle counter. Finally, two external measurement units 17-1 and 17-2 are necessary for intermediate and post-processing measurements to determine whether or not the wafer is still within the specifications at the output of each chamber. As apparent in Fig. 2, the measurements are respectively performed at the output of chambers 11-1 and 11-2. Measurement units and control devices are sometimes provided with a local database to record the main events for subsequent review by the operators at the end of the process. Data bus 18 provides the necessary electrical connection between the computer 12 and the EPD controllers 14-1 and 14-2 for an elementary data exchange. As a matter of fact, the role of EPD controllers is only to signal that the etch end point has been detected or if not, that the processing step has reached the maximum allowed time for that determined step.

[0008] The operation of system 10' is relatively simple. Let us assume that for sake of simplicity, that (1) only three steps labelled A to C are performed in the first chamber 11-1 with only two steps (A and C) monitored by EPD controller 14-1 and (2) only one step (A) is performed in chamber 11-2. First, computer 12 down-loads physical process parameters to chamber 11-1 via data bus 13 the way described above, and in the meantime, the identification number of the algorithm to be used in step A is sent to EPD controller 14-1 via bus 18. Starting step A in chamber 11-1 also starts the EPD controller 14-1 scanning of the selected etch end point parameter, typically a specific radiation wavelength that is emitted by a determined layer at the surface of the wafer. A surge in the signal representing this emission indicates that the end point has been reached. However, other parameters can be used as well. The signal transmitted via optic fiber 15-1 is processed in EPD controller 14-1 to detect the etch end point. In that case, a signal is emitted by EPD controller 14-1 via data bus 18 to inform computer 12 that the etch end point has been reached and that step A must be stopped. In the contrary, EPD controller 14-1 informs computer 12 that the maximum allowed time has been reached. Next, step B is initiated. The duration of this step is not monitored by EPD controller 14-1, so that it is therefore determined by a time fixed by the user. Let us assume that step C is performed the same way as step A, i.e. it is also monitored by EPD controller 14-1. Once step c has been completed, the wafer is sent to the measurement unit 17-1 to check whether or not its complies with the specifications. Only good wafers are loaded in chamber 11-2 to continue processing. Once step A is achieved in chamber 11-2, a new measurement step is performed in measurement unit 17-2. It is important to notice, that none of these steps A to C performed in the first chamber interferes with another, nor with the step performed in the second chamber. In other words, all these steps are sequentially performed without any influence of a previous step on the following step. As mentioned above, during these steps, computer 12 checks all different physical process parameters and stops current process only one of them passes beyond a predefined limit. Optionally, a summary of these physical process parameters can be uploaded in the database of computer 12 for subsequent analysis.

[0009] A better understanding of the complex interactions between the system 10' of Fig. 2 and the wafer fabrication process itself will be best understood by the following description made by reference to Figs. 3 to 5 when the system 10' is used to perform the so-called "AB ETCH"/"AB STRIP" in the course of the trench formation process in DRAM chips. The "AB ETCH" is comprised of three etching steps (labelled A, B and C) performed in sequence in the same chamber, i.e. 11-1 of the etch tool 11. The "AB ETCH" is followed by the "AB STRIP", a single step (labelled A) in chamber 11-2 that aims to remove the photoresist material remaining after these three etching steps. The "AB ETCH/AB STRIP" process has been chosen because it is consistent with the above description made by reference to Fig. 2 but also because it is a good introduction to the method and system of the present invention. Please refer to European Pat. appl. No 756,318 for more details. The "AB ETCH" process will be first briefly summarized hereinbelow.

[0010] Let us consider Fig. 3 which is comprised of Figs. 3A to 3D. Now turning to Fig. 3A, there is shown a portion of a semiconductor wafer illustrating a structure referenced 19 at the initial stage prior to the "AB ETCH" process properly said. Structure 19 to be etched includes a silicon substrate in which shallow trenches 20A and 20B have been selectively formed using an in-situ Si_3N_4 mask layer 21. These trenches are filled with TEOS SiO_2 material by the deposition of a conformal layer 22. At this stage of the fabrication process, small and wide depressions referenced 23A and 23B are formed in layer 22 above trenches 20A and 20B respectively as shown in Fig. 3A. Planarization of structure 19 then requires the successive deposition of two photoresist layers. A photoresist layer (AB1) 24 with a thickness of 830 nm is first deposited onto the structure 22, then exposed, baked and developed as standard to leave a patterned layer referred to as AB1 mask still referenced 24. In essence, the aim of this mask 24 is to fill the wide depressions 23B and a determined amount of small depressions such as 23A. Next, a second 830 nm thick layer (AB2) 25 of the same photoresist is applied over layer 24, then baked. After this second step, we can

consider that the wafer surface is coarsely planar.

[0011] Now, the coarsely planarized surface of the Fig. 3A structure will be transferred to the TEOS SiO2 layer 22 to produce a thinner but substantially planar layer of TEOS SiO2 all over the silicon wafer according to the "AB ETCH" process. The "AB ETCH" process is completed in three different steps labelled A to C. All these steps are achieved in a single chamber of the AME 5000 plasma etcher as mentioned above.

[0012] According to the first step, referred to as step A, the top resist layer 25 is etched until the surface of the TEOS SiO2 layer 22 (at mount locations) is reached. By means of an adequate algorithm, EPD controller 14-1 is used to detect the AB2 layer 25/TEOS SiO2 layer 22 interface, by detecting a SiO ray having a wavelength of 230.0 nanometers.

[0013] Fig. 4 shows the plot displayed on EPD controller 14-1 screen at the end of step A. Curves 26 and 27 respectively show signal S1 which illustrates the 230.0 nm SiO intensity as a function of time during this first step A and its derivative signal S'1. On the other hand, curves 28 and 29 respectively show signal 52 which illustrates the intensity of a CO ray having a wavelength of 483 nm and its derivative signal S'2. Signal S'2 allows to determine the etch rate of AB2 layer 25 as standard. Signals S1 and S2 result from optical measurements. Signals depicted in Fig. 4 are illustrative of a structure 19 without any defect and an etch process perfectly conducted. The surge that can be noticed in signal S'1 (curve 27) is used as the etch end point criteria for step A. A short over-etching is then conducted to terminate this step. At this stage of the process, the structure 19 is shown in Fig. 3B.

[0014] Now, the second step B is performed to remove a given amount (about 160 nm) of the AB1 photoresist and TEOS SiO2 layers with a different non selective etching chemistry. The resulting structure is shown in Fig. 3C.

[0015] In the third and last step C, the TEOS SiO2 layer 22 is etched using the AB1 resist layer as an in-situ mask. To that end, controller 14-1 now performs an interferometric measurement of the type described in European Pat. No 735,565 to Auda et al jointly assigned to IBM Corp. and SOFIE Inst. to determine the etch endpoint. Briefly said, a light beam generated by a mercury lamp is applied to the wafer. According to that reference, two different wavelengths are used to control the amount of TEOS SiO2 layer 22 etched from a given starting point so called "RATE TIME".

[0016] Fig. 5 shows the plot displayed on EPD controller 14-1 screen at the end of step C. Curves 30 and 31 respectively illustrate signals S3 and S4 that are representative of the 404.7 nm and 435.8 nm Hg radiation intensity as a function of time. Curves 32 and 33 illustrate their respective derivative signals S'3 and S'4. Both wavelengths can be used for etch end point determination. The typical shape of curves 30 to 33 are still illustrative of a structure 19 without any defect and of an etch process correctly performed. The sine-shaped curves 30 and 31 allow an easy determination of the etch rates at step C. The reader may wish to consider the Auda et al reference for more details related to this particular measurement technique. At the end of the "AB ETCH" process, the targeted TEOS SiO2 thickness remains over the Si3N4 mask layer 21. The resulting structure is shown in Fig. 3D.

[0017] The interactions between the different constituting parts of system 10' and the "AB ETCH/AB STRIP" process therefore read as follows. First, the wafer to be etched is introduced in chamber 11-1 of the AME 5000 plasma etcher tool 11. Then, the etch process of step A starts, so does EPD controller 14-1. When etch end point is found, step A is stopped. Then, step B is initiated. Once step B is finished after a fixed period of time, step C is completed as described by reference to step A. Finally, after completion of the whole sequence of steps A to C, the wafer is sent (may be true for some sample wafers only) to measurement unit 17-1 in order to determine whether the remaining TEOS layer 22 thickness is within specifications or not. If remaining TEOS layer 22 is too thin, the wafer is rejected. If remaining TEOS layer 22 is too thick, the wafer is sent back to the chamber 11-1 for rework. Reworked wafers are measured again. Good wafers are loaded in a cassette and then sent to chamber 11-2 for stripping the remaining of photoresist AB1 layer 24 according to step A of the "AB STRIP" process. After the "AB STRIP" process has been completed, the wafer is sent to measurement unit 17-2 to check if this step has been satisfactorily performed.

[0018] The above step sequence for a correctly processed wafer may be schematically summarized as follows.

1) Unload wafer from cassette and load wafer in chamber 11-1.
2) Run the three steps A to C of the "AB ETCH" process.
3) Measure the remaining TEOS SiO2 layer thickness in measurement unit 17-1. Dismiss bad wafer for rejection or rework.
4) Load wafer in chamber 11-2.
5) Run the single step A of the "AB STRIP" process.
6) Unload wafer from tool and load wafer in cassette.
6) Perform post-processing check in measurement unit 17-2. Dismiss bad wafer for rejection or rework.
7) Go to the next process.

[0019] The intermediate steps of loading/unloading the wafer into/from the cassette have not been mentioned for sake of simplicity.

[0020] The process flow showing the different processing/measurements steps conducted in their respective tools/equipments is shown in Fig. 6. As apparent from Fig. 6, because the TEOS SiO2 layer

thickness needs to be checked in measurement unit 17-1 before it is sent to chamber 11-2, the "AB ETCH" process cannot be clusterized, i.e. a direct transfer between chambers 11-1 and 11-2 is impossible. In others words, this process cannot be qualified as "in-situ" because the wafer leaves the vacuum of tool 11 for that measurement step. Finally, this sequence of steps terminates by another mandatory measurement step in measuring unit 17-2.

[0021] In addition, using EPD controller 14-1 to control steps A and C does no guarantee a correct "AB ETCH" process. Some serious problems that often occur at this stage of the fabrication process may lead to reject a number of wafers. One can distinguish among these problems, according to a coarse classification, those related to misprocessing errors, process drifts and tool failures. A typical misprocessing error consists to have AB1 or AB2 layer (or both) missing. For instance, if the AB2 layer 25 is missing, the EPD controller 14-1 will wait the occurrence of a transition in the S'1 signal (related to the 230 nm SiO ray) which will never happen. As a consequence, step A will stop at the end of the maximum allowed time. In this case, the wafer must be rejected because during this step, there has been performed an undesired over-etching of the AB1 mask layer 24 and of the TEOS SiO2 layer 22. The wafer is definitely damaged and is no longer reworkable. The other most commonly observed misprocessing errors are: a non-exposure of the AB1 photoresist layer 24, the TEOS SiO2 layer 22 thickness out of specifications or the TEOS SiO2 layer simply missing. A deposition of polymers on the view-port surface of the AME 5000 plasma etcher will produce process drifts that could be detrimental to keep the wafer within specifications. Finally, an electrical misfunction on the buses or a RF shut-down are typical examples of tool failures.

[0022] For these reasons, the "AB ETCH" process needs to be constantly under human control as it is the only way to react if a problem occurs. The operator must periodically adjust parameters in the course of the process depending on its evolution, making thereby very difficult any automation attempt. Moreover, because there is no possibility to intervene during the process, a problem is only detected when a wafer is extracted from a chamber, so that it is too late to save the wafer which is often no longer reworkable. As a matter of fact, with the Fig. 2 system, about 5% of the wafers are rejected at the end of the "AB ETCH" process. Finally, it has also to be noticed that the "AB ETCH" process is slow because the measurement step performed in unit 17-1 necessitates a wafer loading/unloading operation in the cassette before a transfer between the two chambers takes place.

[0023] In summary, none of the system configurations shown in Figs. 1 and 2 is able to react in-line and in real-time to any of the above mentioned problems during the current processing step: wafer misprocessing, process drifts, and tool failures to immediately undertake the right corrective action. Moreover, these system configurations result in non automated tools because no clusterization is possible, so that the wafer processing cannot be performed in-situ in a multi-chamber tool. Mandatory measurement steps slacken the process flow. Consequently, it would be highly desirable to develop a method and a system that would get rid of all these drawbacks.

SUMMARY OF THE PRESENT INVENTION

[0024] It is therefore a primary object of the present invention to provide a method and a system for semiconductor wafer fabrication process real-time in-situ supervision.

[0025] It is another object of the present invention to provide a method and a system for semiconductor wafer fabrication process real-time in-situ supervision that get rid of misprocessing errors, process drifts and tool failures by real-time detection thereof during wafer processing.

[0026] It is another object of the present invention to provide a method and a system for semiconductor wafer fabrication process real-time in-situ supervision that significantly reduce the wafer rejection rate for increased manufacturing yields by stopping the processing or bypassing the next steps while the wafer is still reworkable.

[0027] It is another object of the present invention to provide a method and a system for semiconductor wafer fabrication process real-time in-situ supervision that drastically reduces processing costs and turn-around time.

[0028] It is another object of the present invention to provide a method and a system for semiconductor wafer fabrication process real-time in-situ supervision that obviates the necessity of having a permanent human control for better automation.

[0029] It is still another further object of the present invention to provide a method and a system for semiconductor wafer fabrication process real-time in-situ supervision that can eliminate some standard measurements to speed-up wafer processing.

[0030] It is still another further object of the present invention to provide a method and a system for semiconductor wafer fabrication process real-time in-situ supervision that allows to process only good wafers to avoid unnecessary processing time and wafer waste.

[0031] It is still another further object of the present invention to provide a method and a system for semiconductor wafer fabrication process real-time in-situ supervision that allows a full clusterized (i.e. in-situ) process allowing a direct transfer of the wafer from one chamber to another of the same tool without breaking the vacuum.

[0032] The accomplishment of these and other related objects is achieved by the system and the method of the present invention.

[0033] A preliminary but essential step of the method consists to establish an adequate database. First of all, before establishing the database, for each step of the process, process engineers select one or several process parameters that allow to monitor that step. The database first contains data relative to the evolution of selected process parameters during a determined step of the wafer fabrication process when this step takes place normally and the evolutions of these selected process parameters in case of identified deviations. These identified deviations are based on all the possible causes of wafer rejection known to the process engineers so far. The process engineers define the set of analysis rules that permit to characterize these deviations and establish the corresponding rejection criteria. These rules are coded in the form of algorithms that are also stored in the database. These algorithms are thus adapted to subsequently monitor said selected process parameters during wafer processing and detect any identified deviations. An alert code and an action, still based upon process engineers knowledge, are assigned to each situation and coded the same way in the database. For instance, the current step can be stopped at any time in case of emergency or the next steps by-passed if so required by the alert code. The whole set of alert codes constitutes the alarms of this step in consideration. These operations are performed for each processing step of the wafer fabrication process and for each tool of the manufacturing line wherever possible.

[0034] Now, during a determined step of the wafer processing, the different equipments (EPD controllers, control devices, ...) that continuously monitor the selected process parameters for that step, generates data (e.g. electric signals) that are in-line and in real-time compared with the corresponding data stored in the database by said analysis algorithms. This analysis is performed in a dedicated unit referred to as a supervisor which receives data from said monitoring equipments and has an adequate connection with the database. If an abnormal situation corresponding to an identified deviation is detected, the supervisor emits the alert code to the computer controlling the process tool to flag an alarm and take an immediate and appropriate action, otherwise the process is continued to its normal end.

[0035] As a result, only "good" wafers will be completely processed for higher throughputs. Moreover, this technique allows a total clusterized in-situ wafer fabrication process.

[0036] The novel features believed to be characteristic of this invention are set forth in the appended claims. The invention itself, however, as well as these and other objects and advantages thereof, will be best understood by reference to the following detailed description of an illustrated preferred embodiment to be read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0037]

Fig. 1 shows a conventional system of the prior art for processing semiconductor wafers which is comprised of a two-chamber processing tool and a dedicated computer.

Fig. 2 shows an improved version, still conventional, of the Fig. 1 system which now includes different additional equipments (EPD controllers, control devices, ...) for a more efficient operation.

Fig. 3 which is comprised of Figs. 3A to 3D shows a semiconductor structure undergoing the sequence of steps of the "AB ETCH" process.

Fig. 4 shows the plot of signals displayed by an EPD controller monitoring step A of the "AB ETCH" process in a plasma etcher chamber when the structure is without defect and when the etch process of step A is performed correctly.

Fig. 5 shows the plot of signals displayed by the EPD controller monitoring step C of the "AB ETCH" process in the same chamber when the structure is without defect and when the etch process of step C is performed correctly.

Fig. 6 shows the flow chart of the "AB ETCH/AB STRIP" process when conducted with the Fig. 2 system when the process tool is a plasma etcher.

Fig. 7 shows the novel system according to the present invention wherein a supervisor is now added to the Fig. 2 system.

Fig. 8 shows the plot of signals displayed by an EPD controller monitoring step A of the "AB ETCH" process when the structure enters step A with the AB1 photoresist layer missing.

Fig. 9 shows the plot of signals displayed by the EPD controller monitoring step A of the "AB ETCH" process when the AB1 photoresist layer has not been patterned by any lithographic step.

Fig. 10 shows the plot of signals displayed by an EPD controller monitoring step A of the "AB ETCH" process when the structure enters step A with the AB2 photoresist layer missing.

Fig. 11 shows the plot of signals displayed by the EPD controller monitoring step A of the "AB ETCH" process when there is an undesired polymer deposition onto the plasma etcher chamber view port.

Fig. 12 shows the plot of signals displayed by an EPD controller 14-2 monitoring step C of the "AB ETCH" process when the structure enters step C with a photoresist drop in the middle of the wafer.

Fig. 13 shows the plot of signals displayed by the EPD controller 14-1 monitoring step A of the "AB ETCH" process when there is a RF shut-down of the plasma etcher during the etch process.

Fig. 14 shows the flow chart that summarizes the different steps to create the database according to the method of the present invention.

Fig. 15 shows the flow chart that summarizes the essential steps involved in the real-time in-line novel process flow according to the method of the present invention when applied to any processing step of the wafer fabrication process.

Fig. 16 shows the flow chart of the "AB ETCH/AB STRIP" process when conducted with the Fig. 7 system of the present invention.

DESCRIPTION OF A PREFERRED EMBODIMENT

THE NEW SYSTEM INCLUDING A SUPERVISOR

[0038] The new system referenced 34 is shown in Fig. 7. With regards to the improved system of the prior art depicted in Fig. 2, identical elements bear the same numeral. Turning to Fig. 7, the main differences lie in the addition of a dedicated unit referred to as the supervisor referenced 35 and the suppression of measurement unit 17-1 that is no longer necessary. Measurement unit 17-2 may reveal to be necessary in the case an anomaly has been detected during the process by the supervisor 35 as it will be discussed in more details later on by reference to Fig. 16. Because a direct wafer transfer between chambers 11-1 and 11-2 is now possible, the tool 11 is considered to be fully clusterized, permitting thereby a so-called "in-situ" process. As apparent in Fig. 7, the supervisor 35 includes an internal database, however it should be understood that an external database could be used instead. Supervisor 35 is connected on the one hand to the computer 12 via a bidirectional data bus 36, typically a SECS II link, and on the other hand to EPD controllers 14-1 and 14-2 via bidirectional data bus 37-1 and 37-2 respectively. However, some intelligence can be optionally installed in the EPD controllers if the supervisor has too many tasks to handle. This can be achieved by adding computing and storage capabilities in the EPD controller itself. An electronic card with a microprocessor and a few memory modules would be adequate in all respects. Optionally, control devices 16-1 and 16-2 can be connected to supervisor 35 via data bus 36, so that the supervisor 35 is also able to follow the process evolution as viewed by said control devices and not only by EPD controllers. The supervisor 35 has thus both computing (to process data coming from the EPD controllers and from the database for comparison purposes) and data storage (to lodge the database) capabilities. It is important to remark that computer 12 has the role of controlling the physical process parameters of tool 11 during the wafer processing while supervisor 35 is mainly interested by what happens to the wafer itself.

THE NOVEL METHOD OF SUPERVISION

SETTING-UP A DATABASE

[0039] The method of the present invention requires the preliminary step of creating a database containing first data describing the process evolution not only when it takes place normally but also in case of any deviation thereof. These deviations are based on all the possible causes of wafer rejection identified so far. For each step, the process parameters that are determining for the monitoring of this step are selected. They are monitored to establish the set of correct process data, corresponding to the normal situation, the evolution of which will be used as the reference for the analysis to be subsequently performed according to the method of the present invention. Then, for each potential cause of wafer rejection identified by the process engineers, the same process parameters (or a few of them, those that are the most adapted to that particular deviation) are monitored to understand their drifts with respect to the reference evolution mentioned above. All the data so collected which are representative of the normal situation and of the identified abnormal situations for this step are stored in the database of supervisor 35. In turn, these drifts are analyzed by the process engineers who then define a set of rules, referred to as the analysis rules, wherein the rejection criteria which characterize this deviation with respect to the normal process are defined. These analysis rules are formulated in the form of algorithms and stored in the database. Finally, to each identified deviation corresponds an alert code and an action defined by the process engineers. The alert codes may have different levels of priorities. On the other hand, the actions to be undertaken may be very different depending upon the seriousness of the deviation. The above procedure is repeated for every step of the process in consideration.

[0040] The few following examples will illustrate this preliminary step of creating such a database. For consistency with the introductory part of this application, they all relate to the "AB ETCH" process, so that they will be described by reference to structure 19 shown in Fig. 3.

EXAMPLE I

[0041] As mentioned above, at the initial stage of the

"AB ETCH" process, i.e. step A, photoresist layer AB1 is normally present. The case where structure 19 has no defect is represented by curves 26 to 29 in the graph of Fig. 4. As apparent from Fig. 4, the derivative signal S'1 (curve 27) exhibits a very sharp transient at the end of the step. Now turning to Fig. 8 which illustrates the signals S1, S'1, S2 and S'2 when the AB1 photoresist layer 24 is missing. In this case, the S'1 signal represented by curve 34 has a more gradual slope instead. This difference will be used by the process engineers to distinguish the two cases. To characterize the absence of the AB1 photoresist layer, the following rule has been established: if signal S'1 is higher than 500 (arbitrary units) and lower than 1600 during at least about 25 s, the AB1 photoresist layer is considered missing. Then, the process engineers have examined the consequence of such a situation. If AB1 photoresist layer is missing and step A performed as usual, during steps B and C, the totality of the TEOS SiO2 layer 22 will be etched leading to a major cause of rejection. Therefore, as soon as the AB1 photoresist layer is detected "missing" the etching must be immediately stopped, so that in this case, the alert code is "IMMEDIATE STEP STOP" and the recommended action is to bypass steps B and C in chamber 11-1. In this case, the wafer is reworkable.

EXAMPLE II

[0042] Let us assume that the wafer has not been submitted to the AB1 lithography step. As a result, the two photoresist AB1 and AB2 layers 24 and 25 are present in their totality at the surface of the structure 19 before the wafer is processed at step A. Fig. 9 shows signals S1, S'1, S2 and S'2 in that particular situation. In this case, process engineers have selected signal S'2 of curve 35 which defines the etch rate and thus the etched thickness. The rule specifies that if etched thickness exceeds 10% of the nominal value, the process should be stopped, otherwise it will continue until the maximum allowed time be reached. Because, the etch end point of step A will never occur, the TEOS SiO2 layer 22 will never be etched, this is why the etch process must thus stop without delay. The alert code will be again "IMMEDIATE STEP STOP" and the recommended action is to by-pass steps B and c. In the instant case, the wafer is not damaged, it just needs to be reworked.

EXAMPLE III

[0043] Still another frequent failure that occurs in the manufacturing at the "AB ETCH" level is the absence of the AB2 photoresist layer 25. If AB2 photoresist layer 25 is missing when step A is initiated in chamber 11-1, the chemistry that is currently used at this step, etches both the TEOS SiO2 material of layer 22 and the photoresist material of AB1 layer 24 at the same rate. In a few minutes, the totality of the AB1 photoresist is removed plus a large amount of the TEOS SiO2 material. As a consequence, the wafer needs to be rejected at this stage of the fabrication process. In this case, signal S'1 will be used, and as soon as an interference is detected, which means that TEOS SiO2 material is being etched, the etching is immediately stopped. Fig. 10 shows signals S1, S'1, S2 and S'2 in that particular situation, wherein signal S'1 is represented by curve 36. In this case, the rule iS: starting from RATE TIME RT of signal S'1 for a maximum duration of 120 s, if signal S'1 amplitude raises above 1500 (arbitrary unit) and decreases below 600 and then raises again above 1500, this means that the etch rate is too high. The alert code is "IMMEDIATE TOOL STOP" and the recommended action is thus to stop the plasma etcher tool. In this particular case, all the remaining wafers of the lot undergoing processing are visually controlled to check the presence of the AB2 photoresist layer 25.

EXAMPLE IV

[0044] This example relates to a tool misfunction. It happens sometimes that the chamber inner walls are covered with byproducts (typically polymers) of the chemical reaction produced by the etching. When step A is initiated, these byproducts are etched first, so that the planned etch time defined to fully remove the AB2 photoresist layer 25 reveals to be not sufficient and at the end of step A, the wafer comes out of chamber 11-1 still with an AB2 photoresist coating. The alert code will indicate to the computer that a further etch is necessary. The criteria developed by the process engineers to characterize this situation may be understood in conjunction with Fig. 11. Fig. 11 shows signals S1, S'1, S2 and S'2 corresponding to that situation. The test will be performed on the amplitude of signal S1 represented by curve 37. Two tests are performed at an interval of 60 s, and if the difference in the signal amplitude is greater than 10%, the alert code will indicate that an additional etch of a determined duration must take place.

EXAMPLE V

[0045] During the AB1 or AB2 photoresist deposition, a drop of resist often falls at the center of the wafer forming a local thickness increase. When the wafer will enter in step C, this defect inhibits the etch end point detection so that the wafer is etched the maximum allowed etch time. Fig. 12 shows signals S3, S'3, S4 and S'4 corresponding to that situation. In this case, the rule specifies that if an asymmetry is detected in signal S'3 represented by curve 38, an alert code "STOP AT DEFAULT TIME" is flagged. The recommended action will be to continue the etching during a pre-determined time (default time).

EXAMPLE VI

[0046] When the RF generator stops and restarts immediately, e.g. during step A, the S1 signal falls and rises again. Its derivative signal S'1 goes more abruptly the same way. The surge that is generated causes a false etch end point so that step A is stopped too early. Next, the wafer is processed according to step B. Finally, when the wafer is submitted to step C, a large amount of photoresist AB2 still remain atop the wafer. The step C chemistry being selective, will not etch the TEOS SiO2 material. As a final consequence, if no alarm is flagged during step A, the wafer will exit the step C with an un-attacked TEOS SiO2 layer 22 and it will be rejected after the chem-mech planarization step. Fig. 13 shows signals S1, S'1, S2 and S'2 corresponding to that situation. The curves representing signal S1 and S'1 are referenced 39 and 39' respectively. In this case, the rule defined by the process engineers is: thirty seconds after step A is started, checks signal S1 amplitude, if the variation between two samplings is greater than 5%, an alert code of "IMMEDIATE STEP STOP" should be flagged. The recommended action will still be to by-pass the B and C steps.

[0047] The different operations that lead to the database creation are schematically summarized by the flow chart referenced 40 in Fig. 14. Let us consider the sequence of operations for the first processing step labelled A of a global process which includes a number of steps labelled A to X. Now turning to Fig. 14, the first operation consists to select the right process parameters to monitor step A and establish their evolution during a processing conducted in normal conditions (box 41-A). The evolution of these selected process parameters will be used, as a reference, to supervise the process in-line and in real-time. In this particular case of the "AB ETCH" process, these selected process parameters, at least includes the four signals S1, S'1, S2 and S'2 depicted in Fig. 4. Next, all the possible deviations with respect to normal process conditions are identified and the evolution of said selected process parameters is established for each deviation (box 42-A). Moreover, still for each deviation, analysis rules, including criteria of rejection, are defined to characterize this particular situation (box 43-A). Note that, if several process parameters are used, the supervisor will analyze them in parallel. Then, specific analysis algorithms are developed (box 44-A). As a matter of fact, there is a specific set of algorithms adapted to each step. These algorithms are developed by the process engineers and are clearly within the scope of a man ordinary skilled in the art. An alert code and the recommended action to be taken are assigned to any identified deviation (box 45-A). Finally, this sequence of operations is performed for each step A to X of the global process. All these data are stored in a database (box 46), which is preferably lodged in supervisor 35, although an external database could be envisioned as well. Database thus includes all the pertinent data related to the process parameters addressing their evolution in normal operating conditions and in the identified deviations thereof. Likewise, it includes the analysis rules with their associated rejection criteria, formulated in the form of analysis algorithms. The database further includes the alert codes and the actions to be undertaken that are assigned to each deviation. Because of the obvious flexibility of the above described procedure, the data base may be thus adapted to one or several steps of the wafer fabrication process and to one or several tools of the manufacturing line.

NOVEL PROCESS FLOW

[0048] The novel process flow will be described by reference to Fig. 15 where it bears numeral 47. It is thus applicable to any processing step and to any tool of the wafer fabrication process. For a determined processing step, the wafer is loaded in the specified chamber of the tool (step 48). Then, computer 12 down-loads the step name in the supervisor 35. Now, the processing (e.g. etching, deposition, implantation ...) of the wafer is initiated for the step in consideration and the EPD controller (and/or any control device) that monitors this particular step is activated (step 49). Simultaneously, the supervisor 35 starts the analysis of the selected process parameters by applying the adequate algorithms stored in its database to analyze the corresponding signals generated by the EPD controller according to the analysis rules stored in the database (step 50). As a result, the evolution of the selected process parameters is permanently analyzed. Upon occurrence of any selected process parameter drift, the supervisor 35 tests if any of the rejection criteria set up by the process engineers is met (step 51). It is the role of the analysis algorithms to recognize any identified deviation to the normal process. The analysis and the test are thus performed in-line and in real-time. If an anomaly (i.e. a deviation) is detected, supervisor 35 will provide an alert code to the computer 12, so that the adequate action can be immediately taken (step 52). If none anomaly has been detected by the supervisor 35, the step in consideration is continued until end (step 53). The wafer is then ready to go to the next step (step 54).

[0049] Let consider now, the reduction to practice of the novel process flow 47 of Fig. 15, when applied to the "AB ETCH/ AB STRIP" process.

[0050] When the first wafer enters in chamber 11-1, the step name has been already sent to supervisor 35 by computer 12 and optionally, a part of this information can be sent to EPD controller 14-1 thru bus 18 if there is some intelligence therein. Step A process starts, so does EPD controller 14-1 to generate signals S1, S'1, S2 and S'2, that are immediately processed by the specific analysis algorithms (selected as soon as the step name is down-loaded in the supervisor 35 database). If an anomaly is detected, depending upon the identified

deviation the corresponding alert code is sent to computer 12 to take the appropriate action. A typical action is to by-pass the remaining steps B and C. However, depending upon the seriousness of the deviation, either the process or the tool can be stopped. If no anomaly is detected, the wafer is processed until step A termination.

[0051] Then wafer enters step B. Step B identification is sent to supervisor 35 by computer 12. Step B is not monitored by EPD controller 14-1 unlike step A, its duration is determined by a fixed time. However, supervisor 35 analyses other signals, such as the signal related to the occurrence of a possible general failure (e.g. a RF shut down). If no anomaly is detected, no alarm is flagged. At the end of the step B process, the wafer enters step C. Step C process is conducted the same way, as described above by reference to step A. Processing the wafer in chamber 11-1 is now complete. Wafer is directly transferred to chamber 11-2 to perform the "AB STRIP" process.

[0052] The above step sequence for a correctly processed wafer may be schematically summarized as follows.

1) Unload wafer from cassette and load wafer in chamber 11-1.
2) Run the three steps A to C of the "AB ETCH" process and step A of the "AB STRIP" process in sequence, except if an alarm is flagged. In this case, the next steps are generally by-passed, although sometimes the process or the tool can be stopped.
3) Unload wafer from tool and load in cassette.
4) Perform post-processing check in measurement unit 17-2 if at least one anomaly has been detected. Dismiss bad wafer for rejection or rework.
5) Go to the next process.

[0053] Again, the intermediate steps of loading/unloading the wafer into/from the cassette have not been mentioned for sake of simplicity.

[0054] The flow chart 55 depicted in Fig. 16 allows a pertinent comparison with the one shown in Fig. 6. As apparent from Fig. 16, because the TEOS SiO2 layer thickness does not need to be checked in measurement unit 17-1 before it is sent to chamber 11-2, the "AB ETCH/AB STRIP" process can be fully clusterized, i.e. a direct transfer between chambers 11-1 and 11-2 is now possible. However, the final measurement step that was performed on sample wafers in measuring unit 17-2 is still maintained if an anomaly has been detected (for batch characterization). With state-of-the-art process tools available to date, a failed wafer cannot be extracted from a chamber as soon as it is flagged "failed". At the end of the "AB ETCH/AB STRIP" process, all the wafers are loaded in a cassette, so that if an anomaly has been detected on only one wafer of the lot, a check must be conducted in measurement unit 17-2 to identify the failed wafer. In the future, this measurement step to sort of wafers could be avoided, should process tools be provided with either a marking device (e.g. a laser) to mark the failed wafers or a reading device adapted to read the wafer ID (identification number) so that failed wafers could be easily identified in the cassette without the necessity of making the measurement step mentioned above.

[0055] Finally, the supervisor 35 that now fully controls all the process steps of the "AB ETCH/AB STRIP" process, through EPD controllers 14-1 and 14-2 now guarantees that only good wafers will be completely processed. Moreover, this technique allows a total clusterized (i.e. in-situ) fabrication process. However, unfortunately, failed wafers cannot be identified at the step where a problem has been detected but are loaded with good wafers in the cassette as mentioned above, necessitating thereby a sort to get the good wafers.

Claims

1. Method for real-time in-situ supervision of a determined step of a process for fabricating a semiconductor wafer belonging to a batch of wafers comprising the preliminary steps of:

   a) selecting at least one process parameter that is determining for the monitoring of that determined step;

   b) establishing a database including:

   - the evolution of said selected process parameter in normal operating conditions and in all the deviations thereof identified by process engineers;
   - algorithms representative of the analysis rules defined by process engineers adapted to recognize any such deviation which include rejection criteria for each deviation; and,
   - an alert code for each case of deviation;

   the method further comprising for that determined step, the steps of:

   c) providing:

   - a tool having at least one chamber for processing the wafer at said determined step of the fabrication process;
   - a tool computer to control the physical process parameters of the tool;
   - at least one monitoring equipment, to mon-

itor at least one selected process parameter that is determining for said step;

- a supervisor that is connected through a network to said computer, said monitoring equipment and said database to supervise the process flow for said determined step;

d) introducing the wafer in the tool chamber;

e) starting wafer processing

f) permanently analyzing the evolution of said selected process parameter by the supervisor for comparison with the corresponding data stored in the database to detect in real-time in-situ any deviation that could occur during said determined step; and,

g) continuing wafer processing to normal end if no deviation is detected and in the contrary taking the corrective action defined by the alert code corresponding to the detected deviation.

2. A system for processing a semiconductor wafer having real-time in-situ supervision capabilities according to a determined process comprising:

a) a tool having at least one chamber to perform said wafer processing;

b) a computer for controlling the physical process parameters of the tool;

c) a monitoring equipment for monitoring at least one selected process parameter of the process which takes place in the tool chamber;

d) a database which contains

. the evolution of said selected process parameter in normal operating conditions and in all the deviations thereof identified by process engineers;

. algorithms representative of the analysis rules defined by process engineers adapted to recognize any such deviation which include rejection criteria for each deviation; and,

. an alert code for each case of deviation;

e) supervising means that are connected through a network to the monitoring equipment, the computer and the database that is adapted to:

- (1) compare the data generated by the controller during current wafer processing with the corresponding data stored in the database to detect any deviation to normal operating conditions; and,

- (2) take the corrective action as soon as the alert code is available.

3. The system of claim 2 wherein said monitoring equipment is an EPD controller.

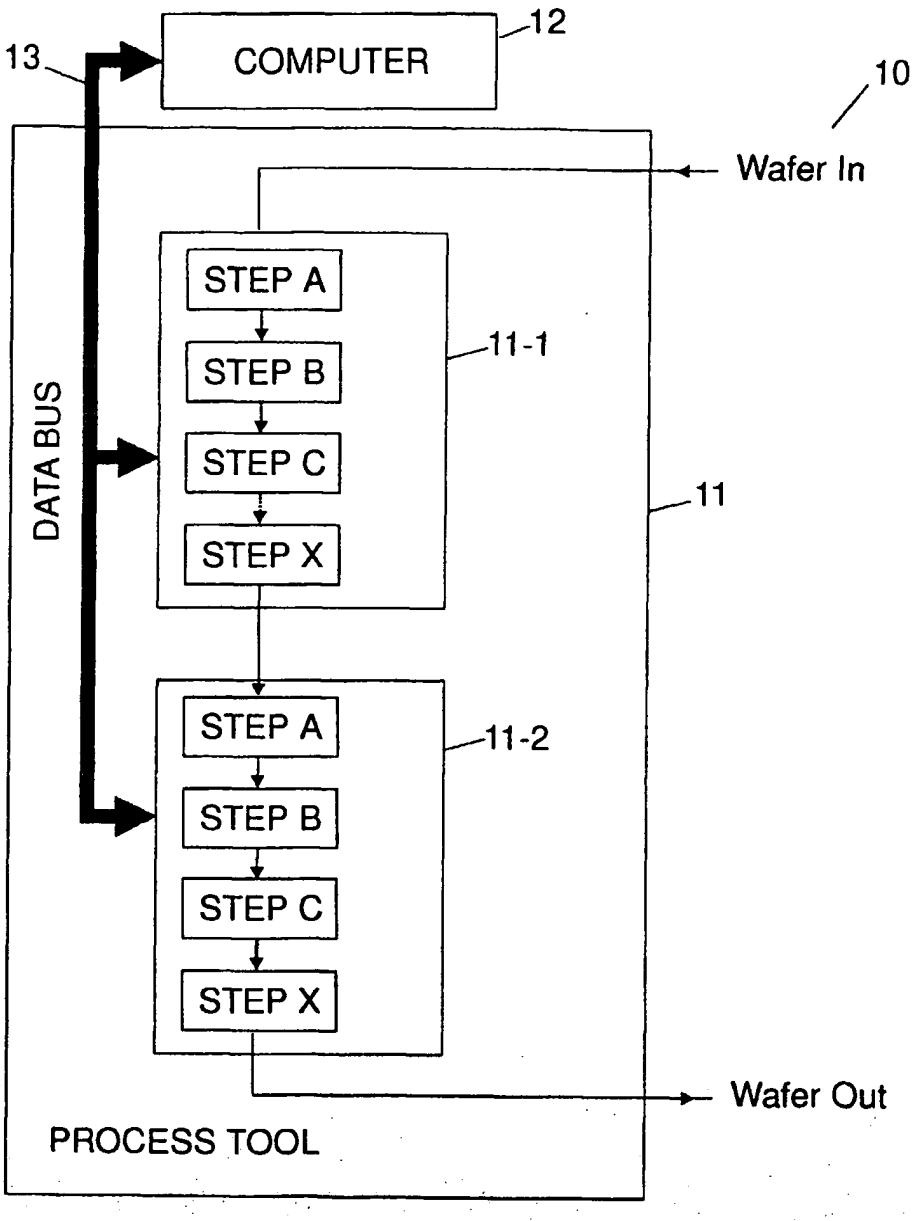

FIG.1
(PRIOR ART)

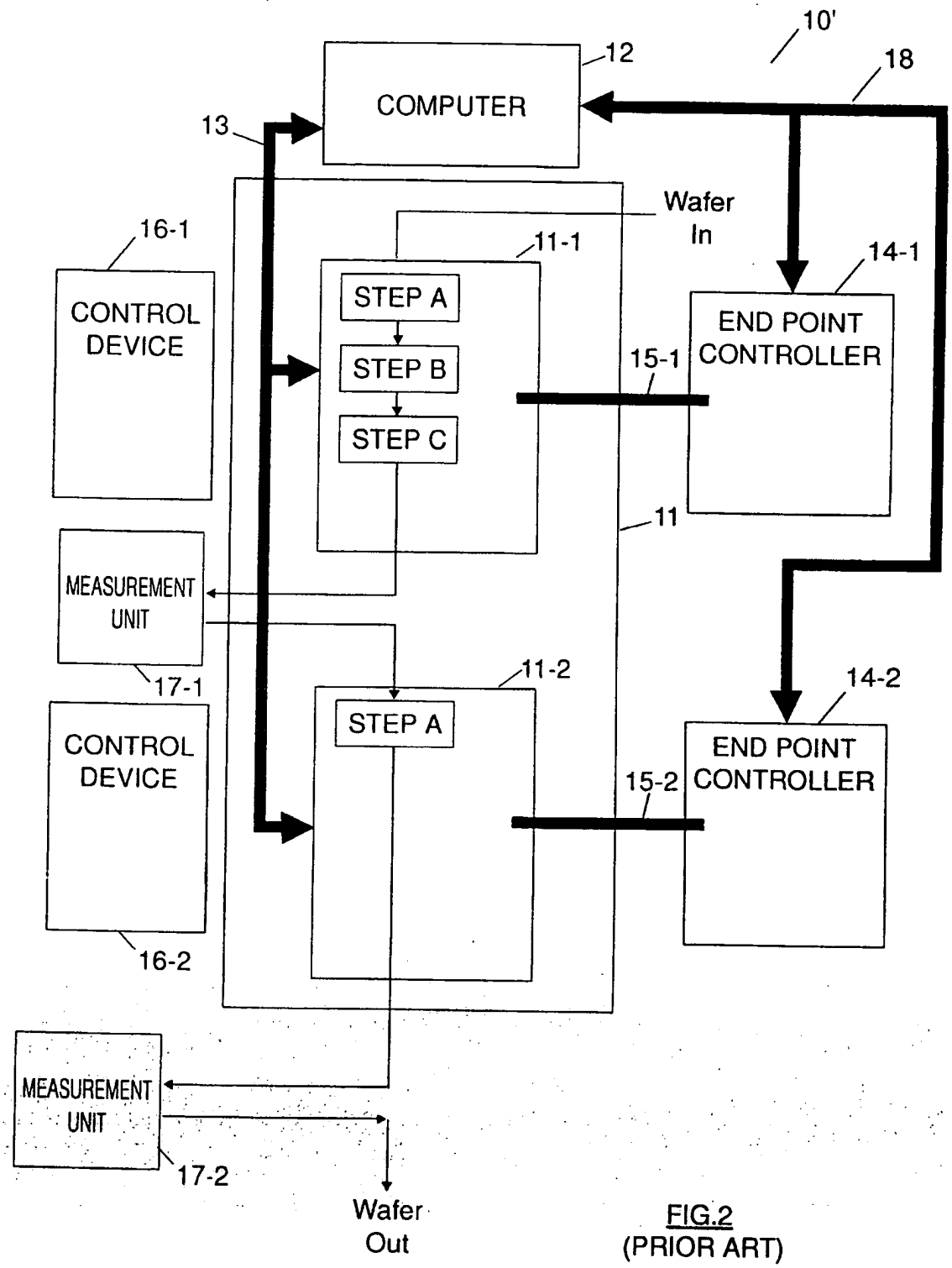

FIG.2
(PRIOR ART)

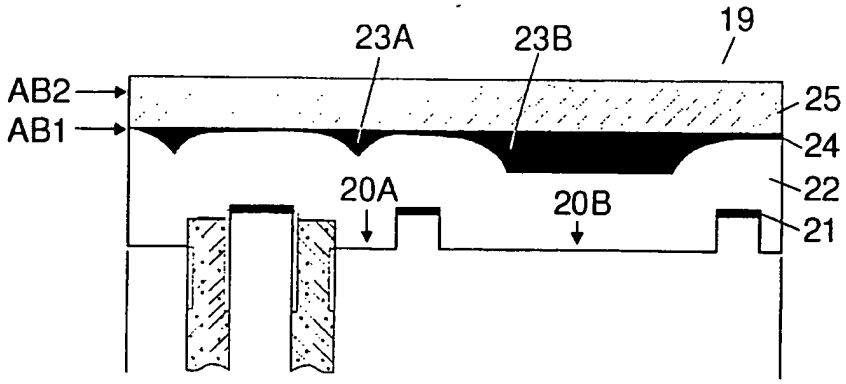

FIG.3A

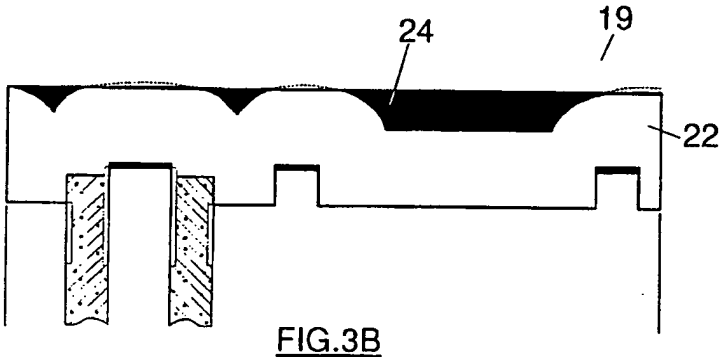

FIG.3B

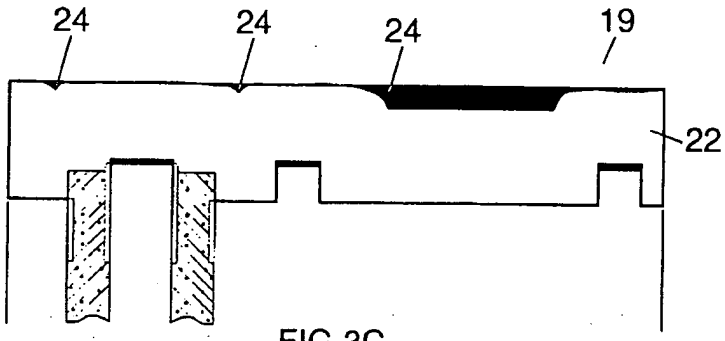

FIG.3C

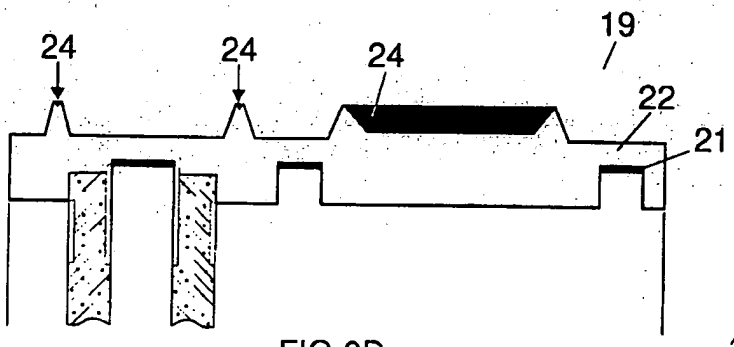

FIG.3D

FIG.3
PRIOR ART

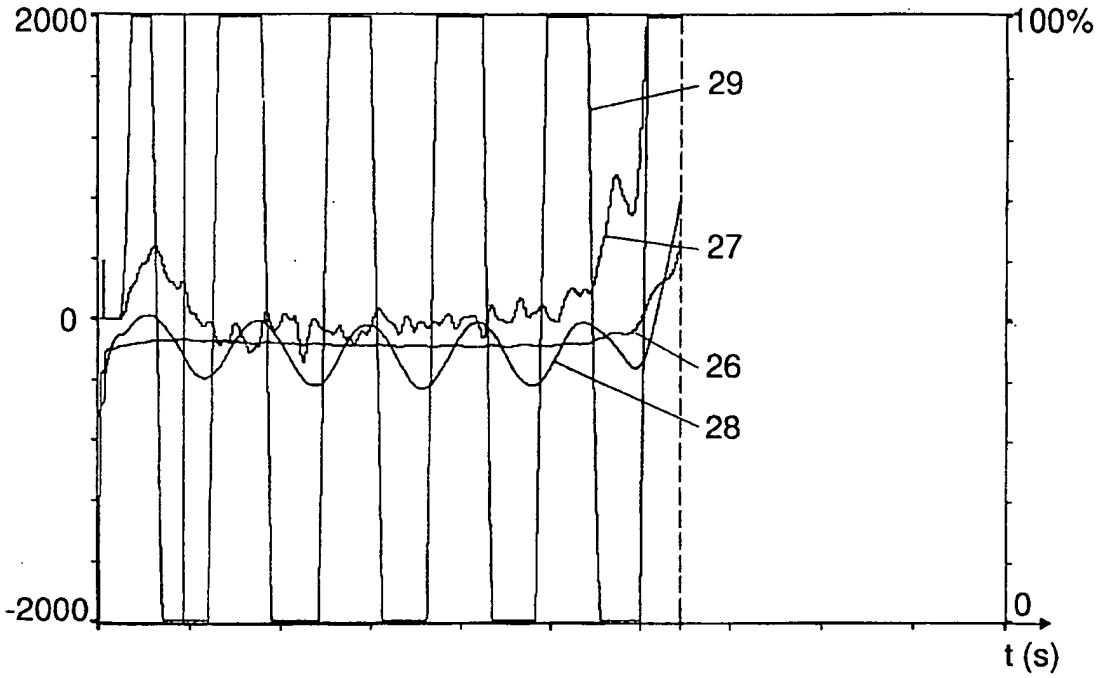

FIG.4

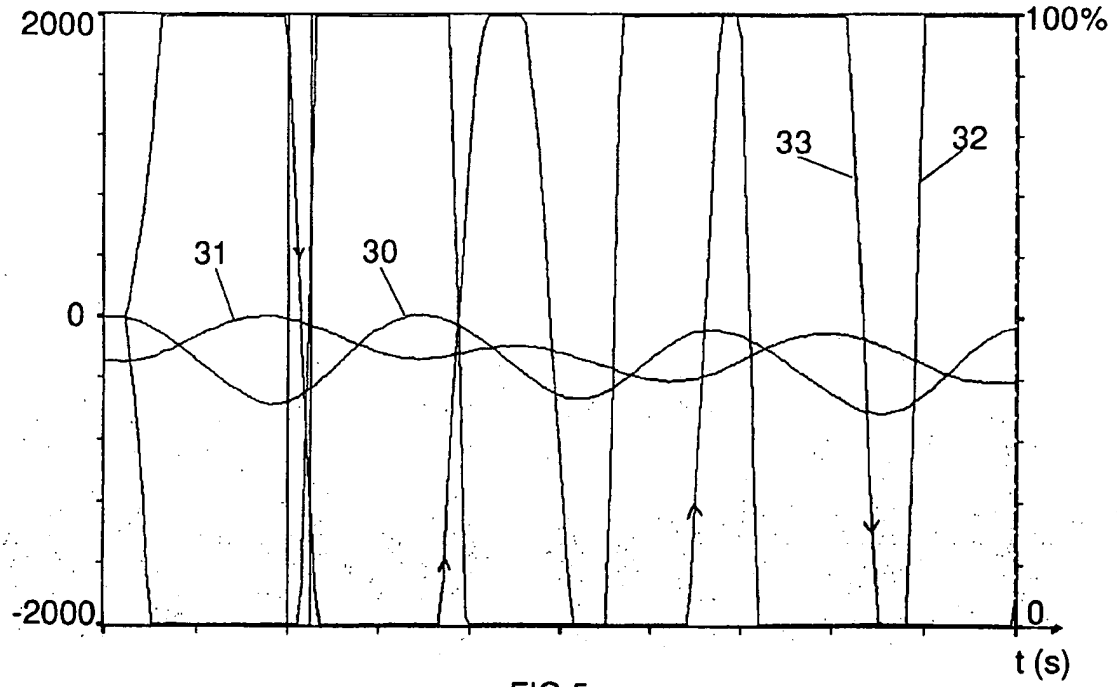

FIG.5

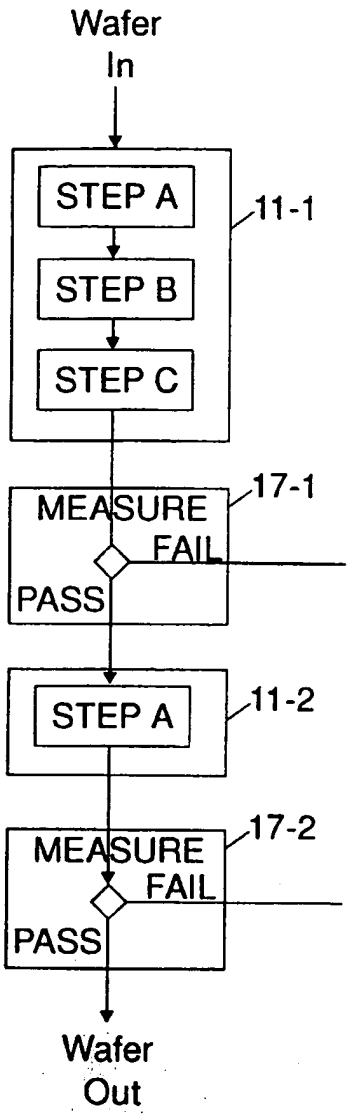

FIG.6
(PRIOR ART)

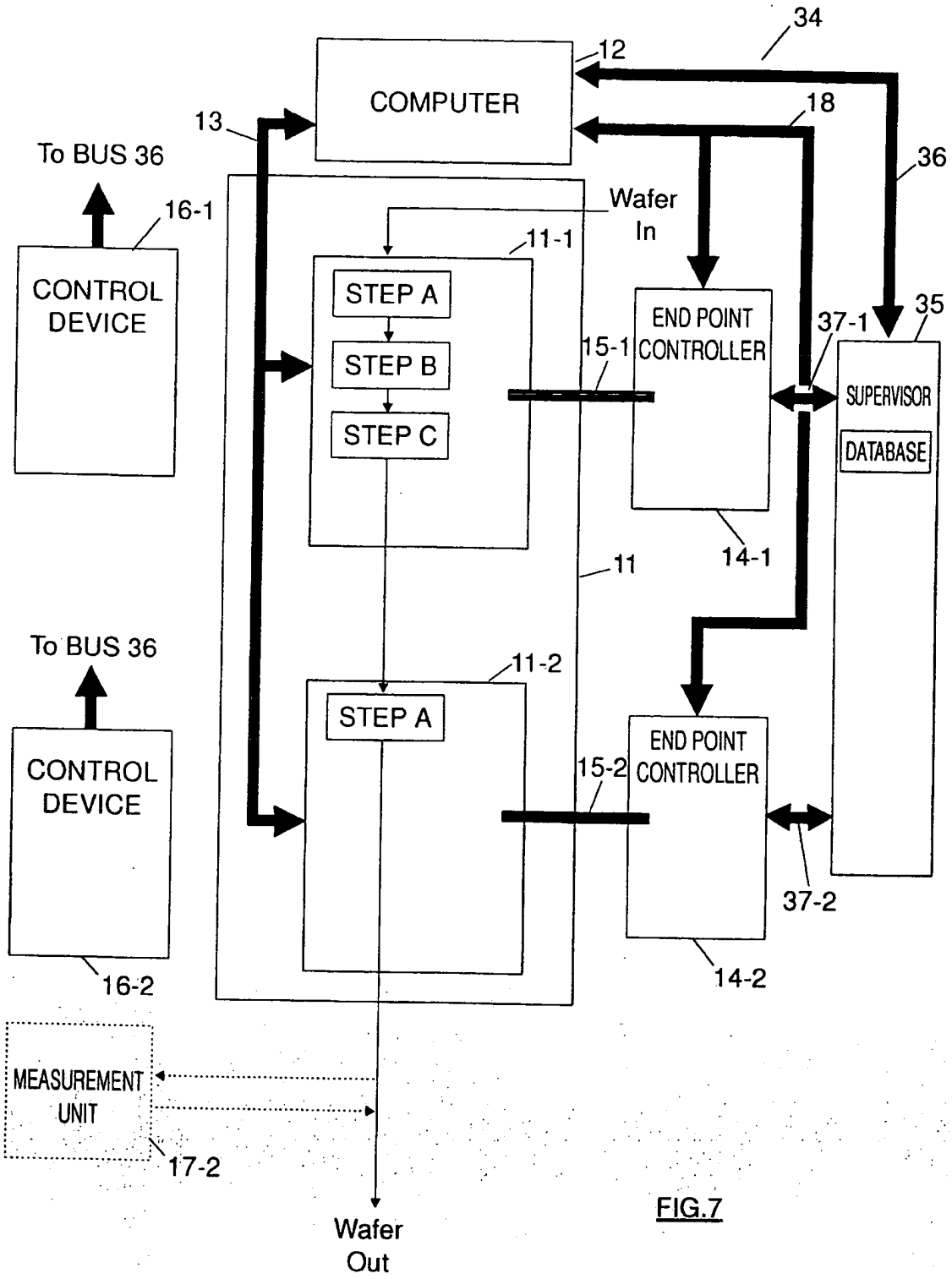
34
12
COMPUTER
13
18
36
To BUS 36
16-1
Wafer
In
11-1
CONTROL
DEVICE
STEP A
STEP B
STEP C
END POINT
CONTROLLER
15-1
37-1
35
SUPERVISOR
DATABASE
14-1
11
To BUS 36
11-2
STEP A
CONTROL
DEVICE
END POINT
CONTROLLER
15-2
37-2
16-2
14-2
MEASUREMENT
UNIT
17-2
Wafer
Out

FIG.7

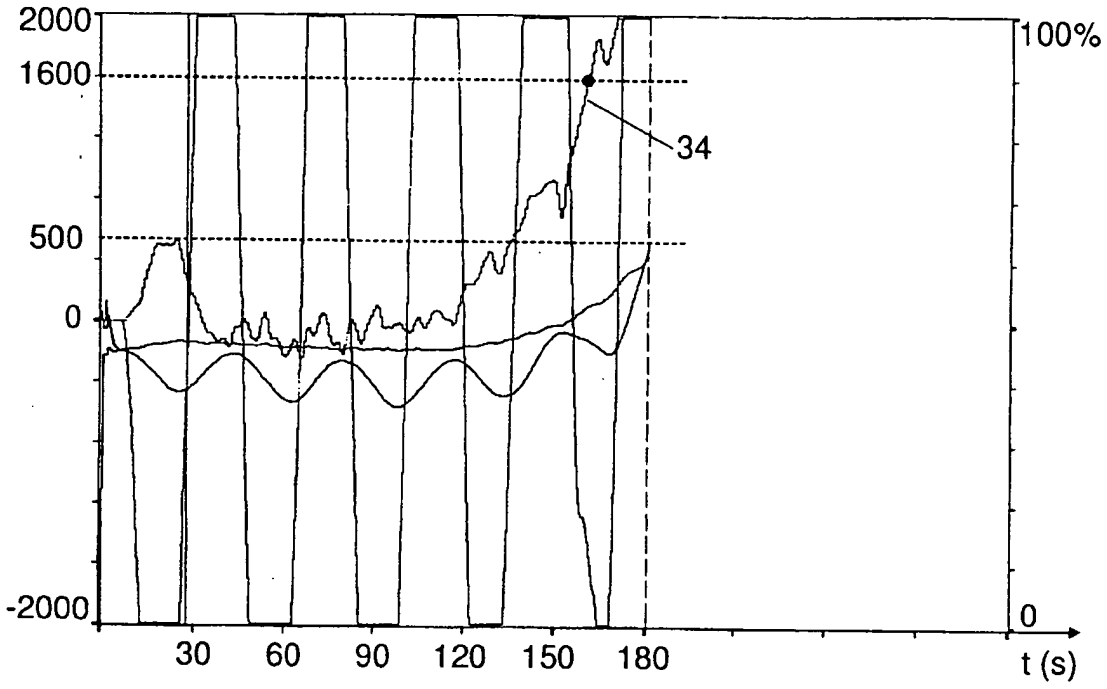
2000
1600
500
0
-2000
100%
0
34
30
60
90
120
150
180
t (s)

FIG.8

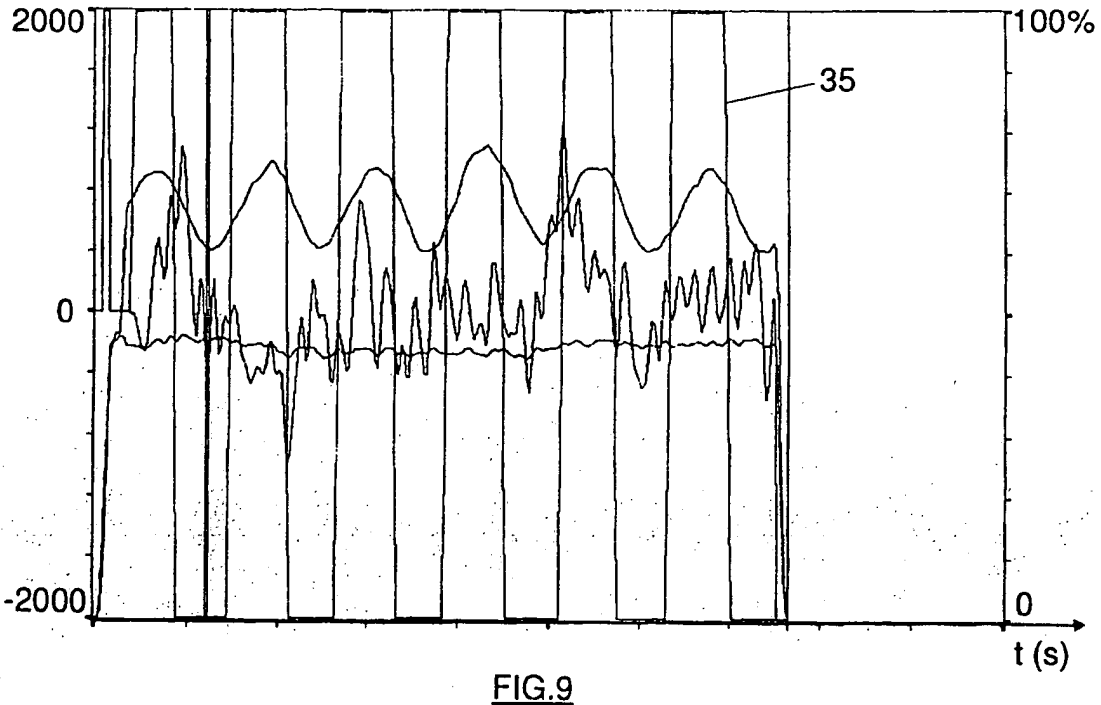
2000
0
-2000
100%
0
35
t (s)

FIG.9

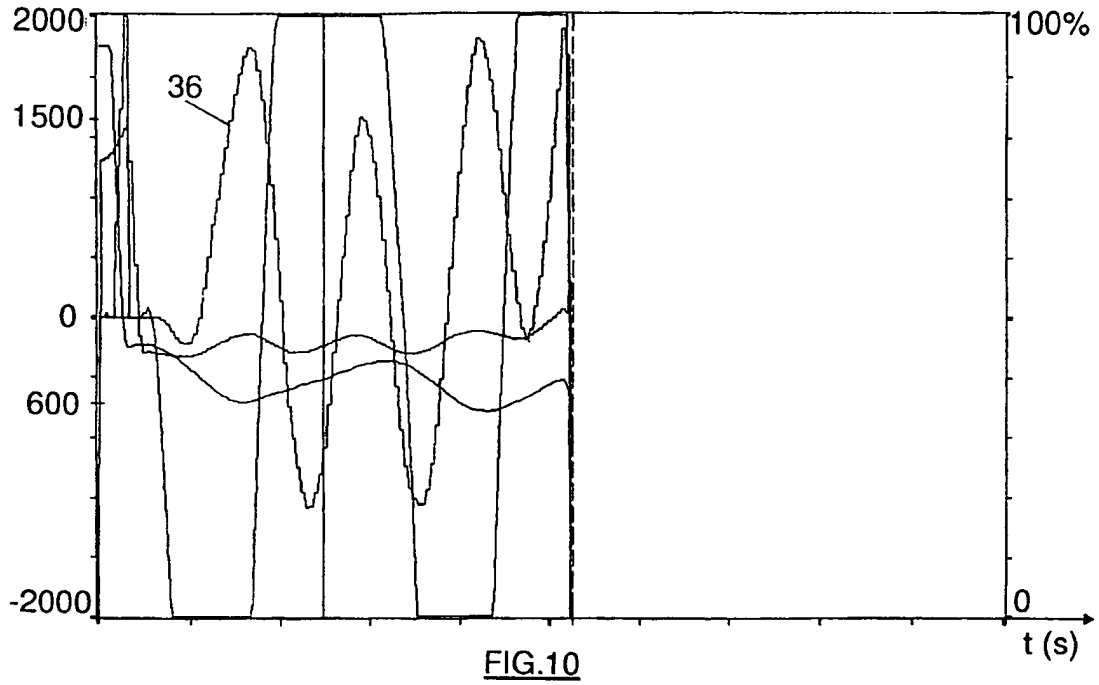
2000
1500
0
600
-2000
36
100%
0
t (s)

FIG.10

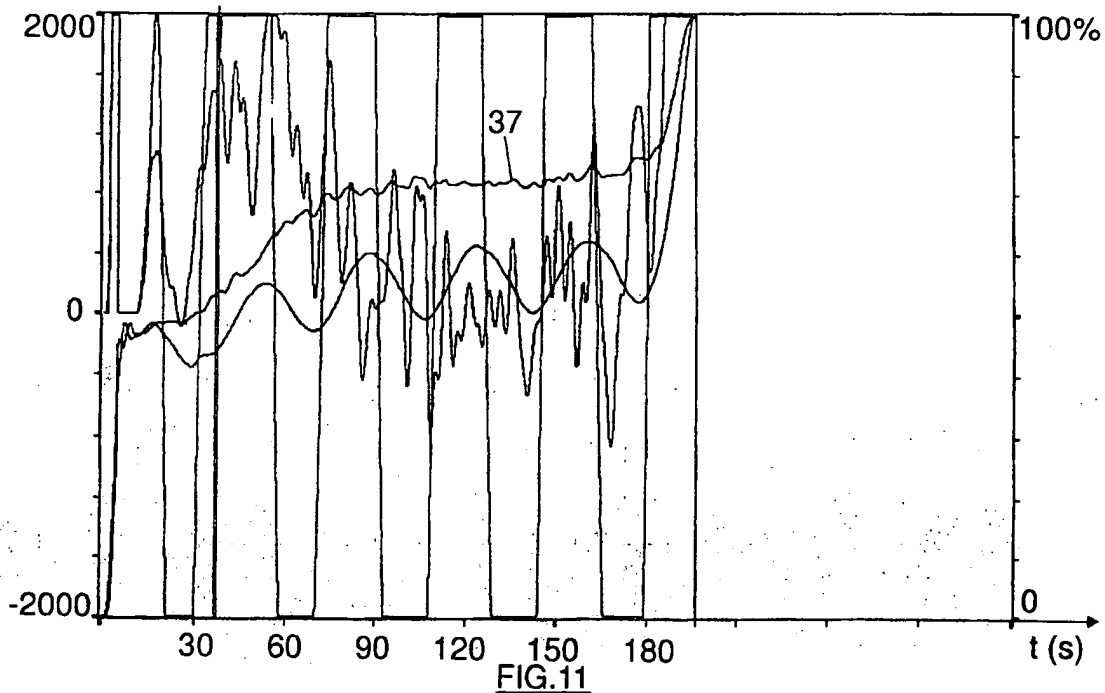
2000
0
-2000
37
100%
0
30
60
90
120
150
180
t (s)

FIG.11

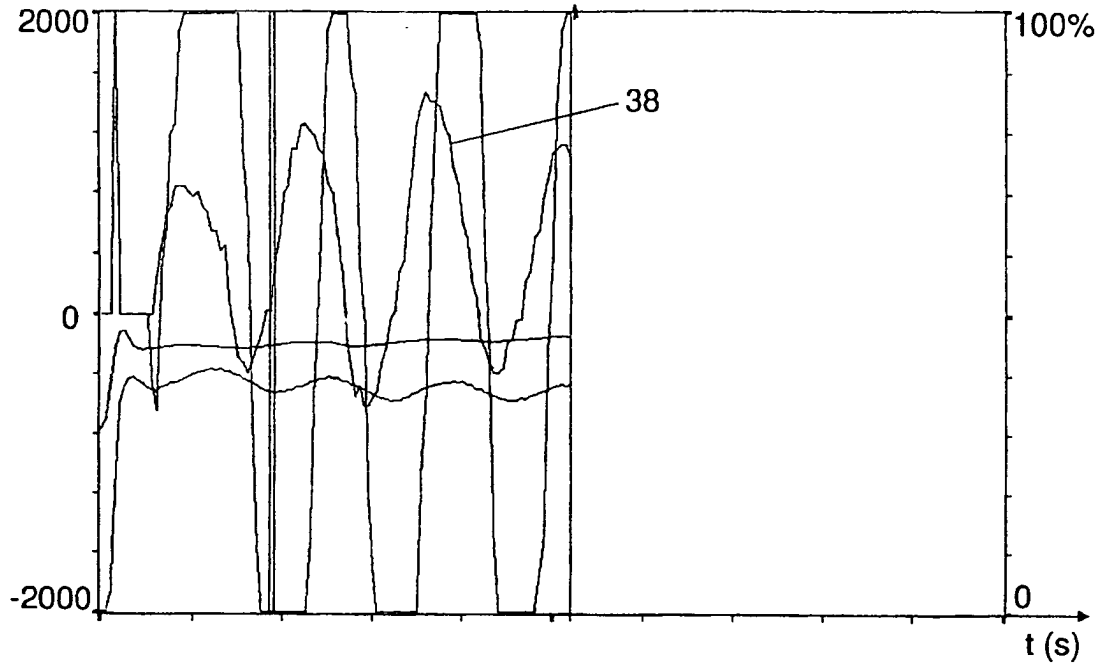

FIG.12

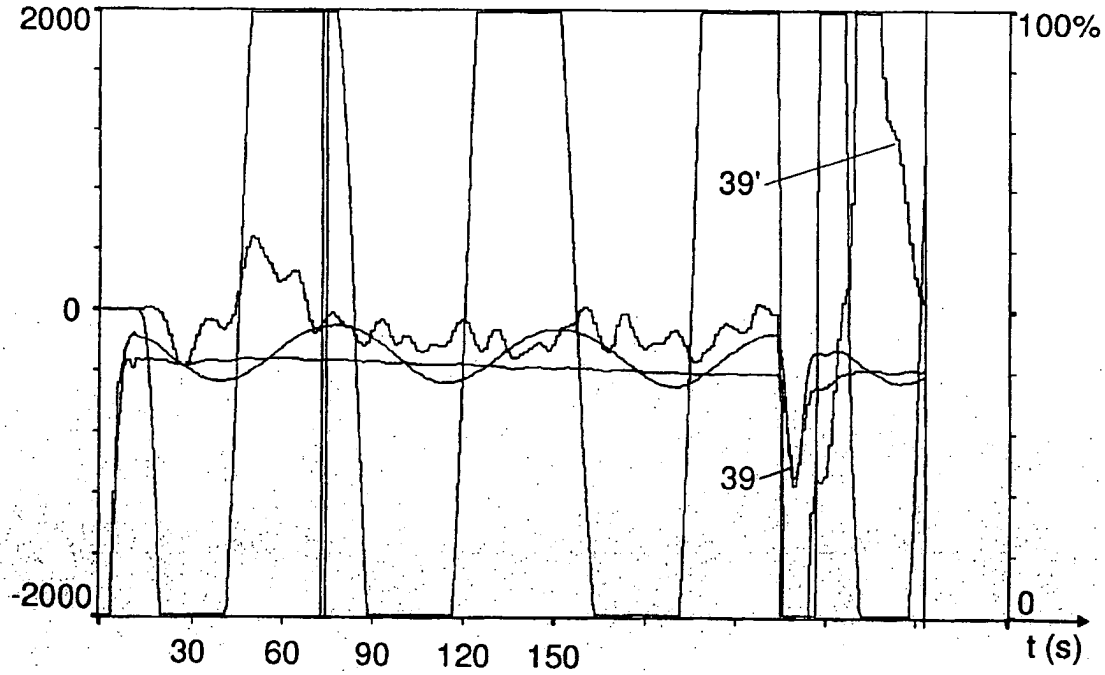

FIG.13

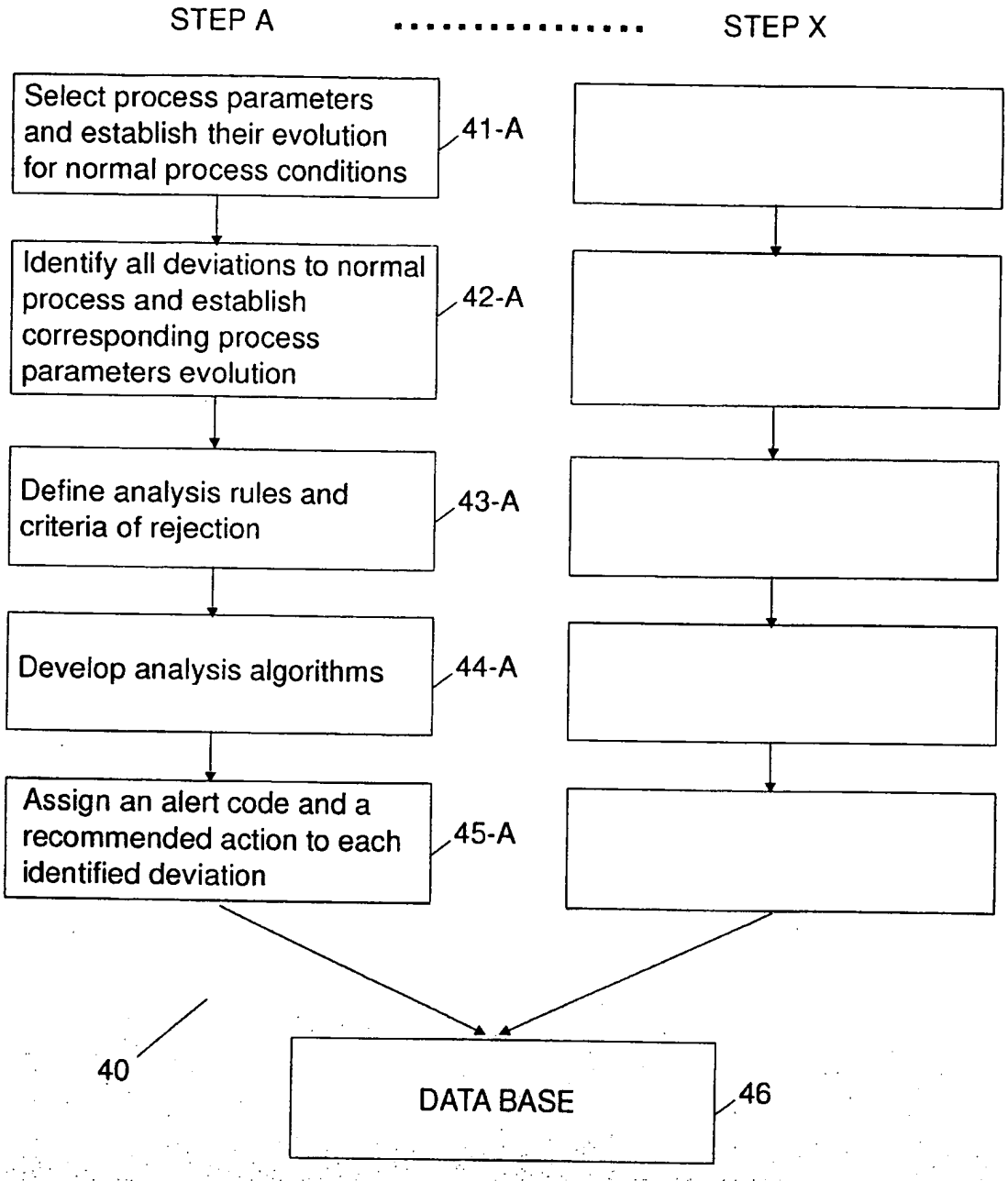
STEP A
STEP X
Select process parameters and establish their evolution for normal process conditions
41-A
Identify all deviations to normal process and establish corresponding process parameters evolution
42-A
Define analysis rules and criteria of rejection
43-A
Develop analysis algorithms
44-A
Assign an alert code and a recommended action to each identified deviation
45-A
40
DATA BASE
46

FIG.14

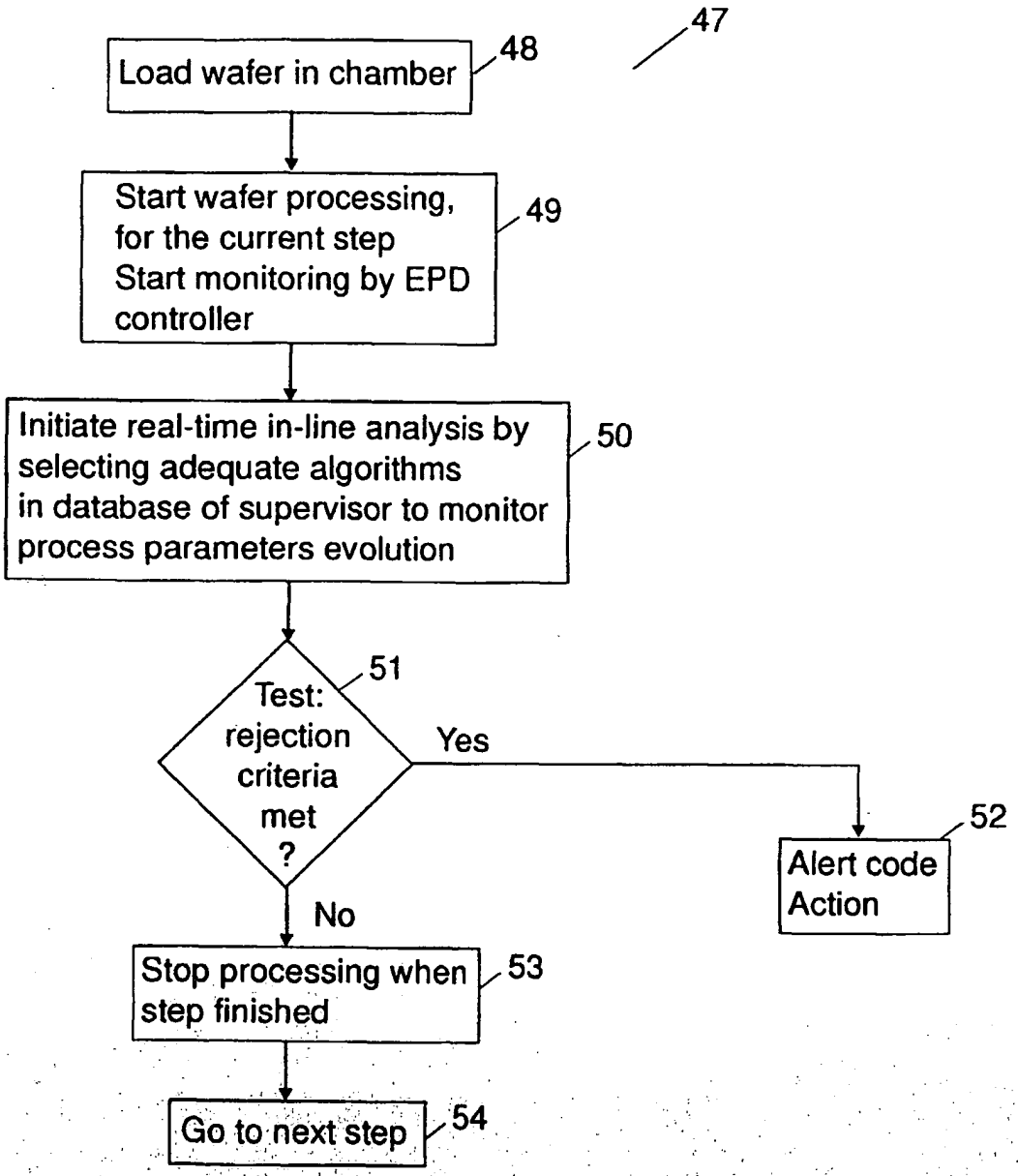
47
Load wafer in chamber
48
Start wafer processing, for the current step Start monitoring by EPD controller
49
Initiate real-time in-line analysis by selecting adequate algorithms in database of supervisor to monitor process parameters evolution
50
Test: rejection criteria met ?
51
Yes
No
Alert code Action
52
Stop processing when step finished
53
Go to next step
54

FIG.15

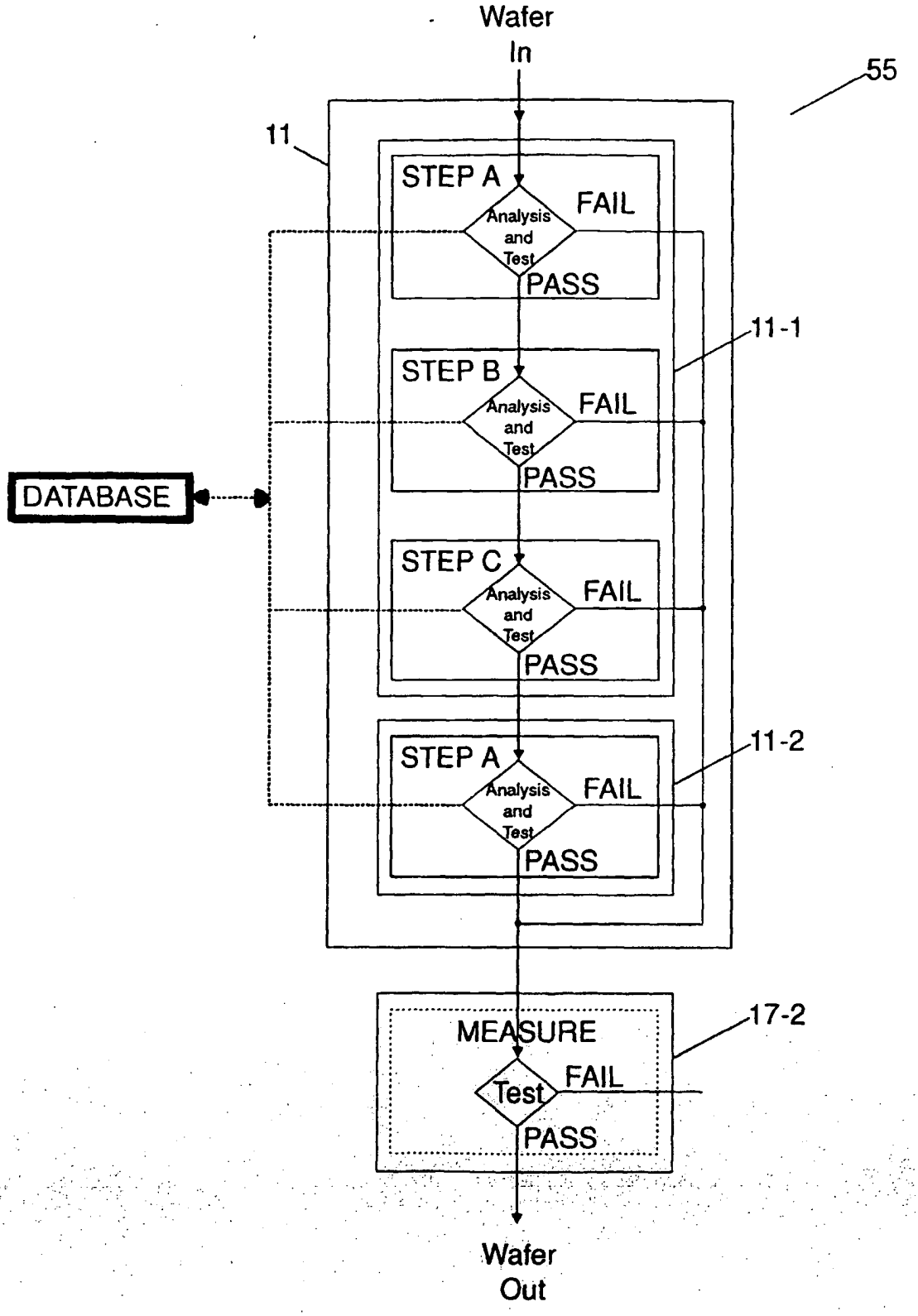
Wafer
In
55
11
STEP A
Analysis
and
Test
FAIL
PASS
11-1
STEP B
Analysis
and
Test
FAIL
PASS
DATABASE
STEP C
Analysis
and
Test
FAIL
PASS
11-2
STEP A
Analysis
and
Test
FAIL
PASS
17-2
MEASURE
Test
FAIL
PASS
Wafer
Out

FIG.16

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 48 0108

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	HU A ET AL: "CONCURRENT DEPLOYMENT OF RUN BY RUN CONTROLLER USING SCC FRAMEWORK" PROCEEDINGS OF THE IEEE/SEMI INTERNATIONAL SEMICONDUCTOR MANUFACTUR SCIENCE SYMPOSIUM (ISMSS), SAN FRANCISCO, JULY 19 - 20, 1993, no. SYMP. 5, 19 July 1993, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 126-132, XP000475399 * the whole document * ---	1-3	H01L21/66
X	WATTS BUTLER S ET AL: "SUPERVISORY RUN-TO-RUN CONTROL OF POLYSILICON GATE ETCH USING IN SITU ELLIPSOMETRY" IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING, vol. 7, no. 2, 1 May 1994, pages 193-201, XP000453332 * the whole document * ---	1-3	
X	"AUTOMATIC PARAMETER WARNING SYSTEM" IBM TECHNICAL DISCLOSURE BULLETIN, vol. 35, no. 6, 1 November 1992, pages 75-77, XP000314069 * the whole document * ---	1,2	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L
A	EP 0 720 074 A (ITT IND GMBH DEUTSCHE) * the whole document * ---	1-3	
A	US 5 625 816 A (BURDICK RANDY ET AL) * the whole document * ---	1-3	
A	GB 2 126 374 A (NIPPON ELECTRIC CO) * the whole document * ---	1-3	
A	US 4 901 242 A (KOTAN NORIHIKO) * the whole document * --- -/--	1-3	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	8 May 1998	Prohaska, G

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Application Number
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DOCUMENTS CONSIDERED TO BE RELEVANT

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A	US 5 511 005 A (ABBE ROBERT C ET AL) * the whole document *	1-3	
A	US 5 483 636 A (SAXENA SHARAD) * the whole document *	1-3	
A	STEFANI J A ET AL: "DIAGNOSTIC MONITORING OF PHOTORESIST ASHING" PROCEEDINGS OF THE IEEE/SEMI INTERNATIONAL SEMICONDUCTOR MANUFACTUR SCIENCE SYMPOSIUM (ISMSS), SAN FRANCISCO, JULY 19 - 20, 1993, no. SYMP. 5, 19 July 1993, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 27-32, XP000475390 * the whole document *	1-3	
A	US 5 210 041 A (KOBAYASHI TSUNEO ET AL) * the whole document *	1-3	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)

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